Dip-Pen Nanolithography of Electrical Contacts to Single Graphene Flakes

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ABSTRACT This study evaluates an alternative to electron-beam lithography for fabricating nanoscale graphene devices. Dip-pen nanolithography is used for defining monolayer graphene flakes and for patterning of gold electrodes through writing of an alkylthiol on thin films of gold evaporated onto graphene flakes. A wet gold etching step was used to form the individual devices. The sheet resistances of these monolayer graphene devices are comparable to reported literature values. This alternative technique for making electrical contact to 2D nanostructures provides a platform for fundamental studies of nanomaterial properties. The merits of using dip-pen nanolithography include lack of electron-beam irradiation damage and targeted patterning of individual devices with imaging and writing conducted in the same instrument under ambient conditions.

KEYWORDS: gold electrode · patterning · graphene · scanning probe lithography · dip-pen nanolithography · nanofabrication

Scaling issues with Si field-effect transistors, particularly charge leakage due to quantum mechanical tunneling,[1] motivate the search for alternative semiconductors that are compatible with nanoscale Si technology platforms and that provide higher carrier mobilities. A material that holds much potential for next-generation nanoelectronics is graphene, which exhibits room-temperature mobility of up to ∼10 000 cm^2/V · s.[2] Moreover, when graphene is patterned into nanoribbons, the carriers are confined to a quasi-1D system, thereby opening a band gap that increases with decreasing ribbon width. Therefore, it is possible to engineer the energy gap of graphene nanostructures for semiconducting applications.[3] Besides being of interest for fundamental studies,[4,5] graphene has been applied in field-effect transistors,[6,7] chemical sensors,[8,9] transparent electrodes,[10,11] and as an electron-acceptor material[12,13] in photovoltaic devices.

The conventional method of fabricating nanoscale devices to explore the unique properties of graphene for electronic applications is electron-beam lithography (EBL).[14] However, exposure to electron irradiation may damage the graphene.[15] This study evaluates dip-pen nanolithography (DPN) as an alternative technique for fabricating these electrical contacts. DPN is a scanning probe-based technique that combines the advantages of EBL (nanoscale resolution) and microcontact printing (direct write).[16,17] In DPN, an AFM probe is dipped into a molecular ink and used to write functional nanoscale patterns. A previous report has already demonstrated DPN of electrical contacts to single carbon nanotubes, with performance of resultant devices comparable to those fabricated *via*

EBL on solution-processed carbon nanotubes.[18] In the case of graphene, using DPN to define nanoribbons and other arbitrary nanostructures bypasses the registration limits associated with using a positive resist in EBL. The goals of this study include evaluating the translation of the DPN process from the 1D carbon nanotube system to the 2D graphene system and characterizing the performance of the resultant devices. The mild processing conditions (lack of electron irradiation) and ease of use and accessibility of AFM systems (as compared to EBL) are strong potential advantages of the DPN approach toward nanodevice fabrication.

The fabrication steps are illustrated in Figure 1. Since the bulk of this study dealt with exfoliated graphene, DPN replaced two EBL steps: (1) etching these multilayer flakes to isolate monolayer graphene and (2) defining electrical contacts. For the first step, a 10 nm film of Au was thermally evaporated onto graphene exfoliated on SiO$_2$. This film was thin enough to allow lateral force microscopy (LFM) imaging of the monolayer graphene underneath, yet still thick enough to be conductive. Next, DPN
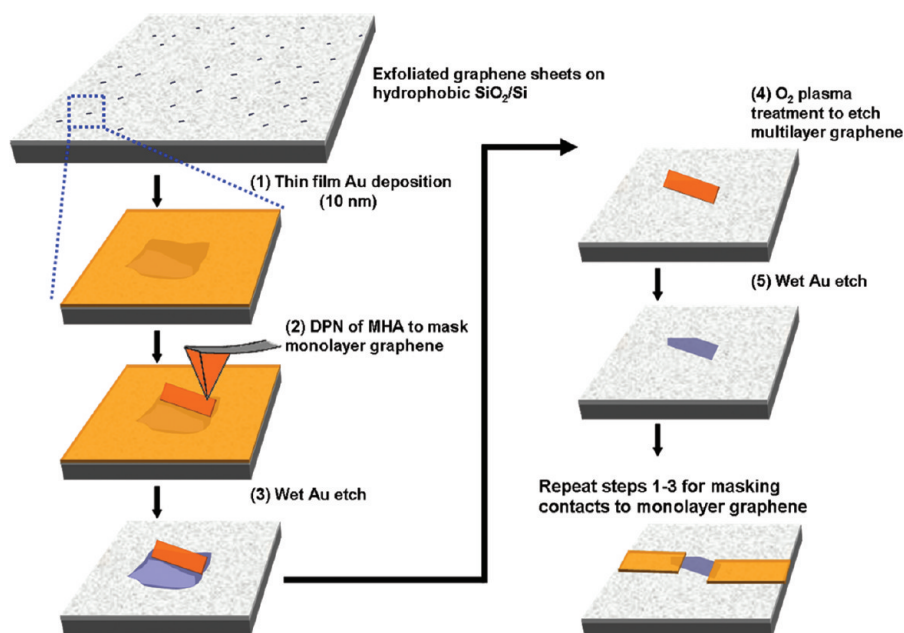
Figure 1. Schematic of graphene device fabrication. The graphene flake shown in step 2 consists of multilayer (lighter) and monolayer (darker) regions. The multilayer regions are exposed and etched away in steps 3 and 4, respectively, leaving behind the monolayer graphene shown in step 5.

of 16-mercaptohexadecanoic acid (MHA) masked the Au[19,20] on top of monolayer graphene, leaving the rest of the multilayer graphene flake exposed after Au etching. An O_2 plasma treatment was then used to etch away the exposed graphene layers.[21] Furthermore, the O_2 plasma removed the MHA mask, leaving the Au film susceptible to wet etching, thereby revealing the isolated monolayer graphene. The second DPN masking step to define nanoscale electrical contacts bridging the graphene flake and the macroscale electrodes was similar to that reported for carbon nanotube device fabrication,[18,22] with the important exception and challenge of having to align the macroscale electrodes *via* a flexible shadow mask. Since only one monolayer flake usually was found and defined per substrate due to the low yield of the exfoliation step, it was necessary to position the macroscale electrodes such that the graphene flake lay within the gap region. The resultant devices were evaluated with AFM and electrical testing to determine whether any damage was inflicted on the graphene during processing.

RESULTS AND DISCUSSION

First DPN Step: Isolation of Monolayer Graphene. DPN was used to isolate monolayer from multilayer graphene in exfoliated flakes. These monolayer regions were identified using optical microscopy and Raman spectroscopy and were matched to the LFM image of the flake under the Au thin film (Figure 2). The area to be masked by DPN using MHA was then designed. The results of subsequent MHA masking, O_2 plasma etching of exposed multilayer graphene, and Au etching to reveal the monolayer flake are shown in Figure 3. It is important to note that the graphene flake remains in the same location on the substrate after solution processing (two Au etches and rinsing steps) due to functionalization of
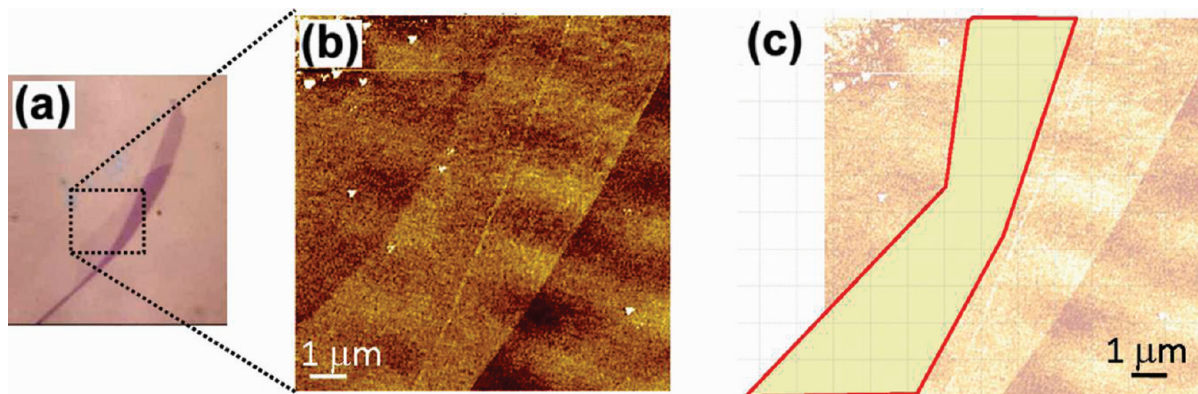

Figure 2. (a) Optical image of graphene flake before Au deposition. (b) LFM image of the flake under 10 nm of an evaporated Au thin film. (c) Registration of MHA mask on the monolayer region. The diagonal ripples in (b) and (c) are scan artifacts due to laser reflection on the substrate.

Figure 3. Optical images of MHA-masked monolayer graphene (pink area indicated by an arrow) after (a) Au etching, (b) O$_2$ plasma etching of exposed graphene layers, and (c) Au etching to reveal the protected flake within the dotted black rectangle. The pairs of blue squares are alignment markers.

the SiO$_2$ substrate with a hydrophobic adhesion layer (dodecyltriethoxysilane).

Second DPN Step: Fabrication of Electrical Contacts. For making contact to monolayer graphene flakes, a new 10 nm layer of Au was deposited on the flake for DPN and one of two routes was taken: (1) parylene-C mask alignment to the flake (Figure 4a), followed by another deposition of macroscale Au contacts and DPN masking of nanoscale electrical contacts, or (2) DPN masking of nanoscale electrical contacts, followed by Au etching and alignment of parylene-C masks (Figure 4c) for deposition of macroscale Au contacts. These conformal parylene-C masks allowed for definition of channel lengths only down to 5 μm,[23] necessitating the use of DPN to bridge between the nanoscale graphene flake and shadow-mask-defined contacts.

In the first route, it was found that the thickness of Au deposited through the parylene-C shadow masks had to be limited to below 25 nm. Any thicker Au films delaminated under Au etching after a few minutes. This effect is presumably due to the lack of an adhesion layer between the Au film and the SiO$_2$ substrate, allowing for the mechanical stress of flow to peel off relatively high aspect ratio Au patterns. This limitation was not present during the previously reported DPN patterning of electrical contacts to carbon nanotubes due to use of an amino-silane-functionalized SiO$_2$ substrate, where the amine groups could bind to Au. Therefore, one could likely circumvent this Au thickness limitation by treating the substrate with an amino silane after the O$_2$ plasma step. Regardless, the first fabrication route still leaves the unmasked Au electrodes vulner-
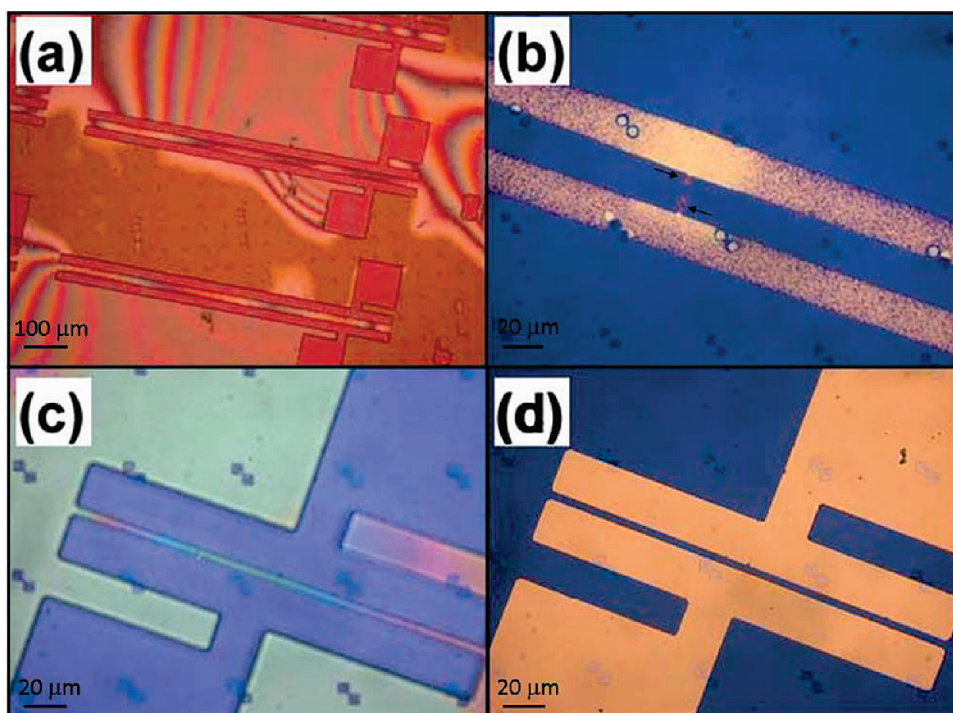
Figure 4. Optical images of two devices fabricated *via* different routes. Device 1: (a) parylene-C mask on top of a 10 nm Au film and aligned to a monolayer graphene flake, (b) final device structure after DPN masking and Au etching of substrate shown in (a). Device 2: (c) parylene-C mask aligned with MHA-masked contacts to monolayer graphene, and (d) final device structure with parylene-C masked contacts intact. Due to its small area, the monolayer graphene flake can only be seen clearly in AFM images. In panel (b), the flake is between the DPN-defined nanoscale contacts (shown in pink and indicated by the arrows).
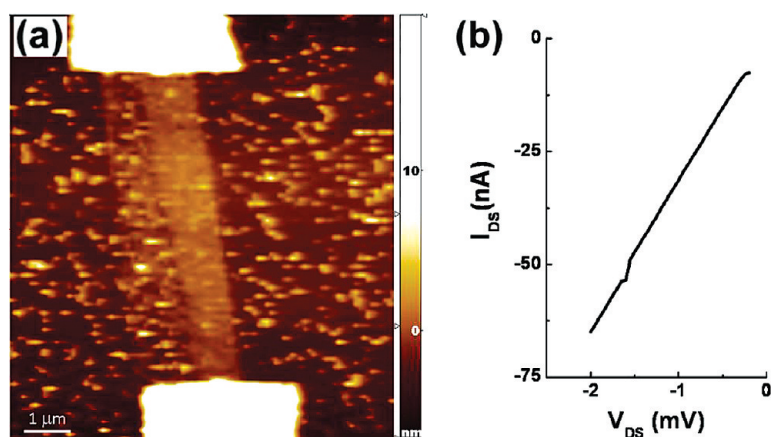
Figure 5. (a) AFM topography image of DPN-generated graphene device. (b) Corresponding $I-V$ curve for $V_G = 0$ V.

able to degradation during the Au etching step to define the graphene device. Figure 4b shows a device in which the macroscale Au electrodes have become pitted during etching.

To prevent degradation of these electrodes, a second fabrication route was developed in which the Au etching to define the graphene device is done before the macroscale Au contact pads are deposited. This second route has the advantage of not exposing the larger Au contacts to etching, thereby enabling the contacts to be an arbitrary thickness greater than 25 nm and ensuring their integrity (Figure 4d). Another advantage is enabling longer Au etching times to eliminate unmasked Au residue since MHA-masked Au is very robust under several minutes of extra etching. A disadvantage, however, is decreased flexibility in placement of the parylene-C mask (smaller margin for error) since the locations of the DPN-patterned contacts are already defined.

Preliminary Electrical Characterization of Monolayer Graphene Devices. A representative graphene device fabricated *via* the first route described in the previous section is shown in Figure 5 along with its $I-V$ characteristics at room temperature in air. There is residual Au on the substrate due to shorter etching times so as not to de-

grade the larger, unprotected Au contacts. Moreover, DPN overmasking of the SiO_2 region to the left of the flake during the isolation of monolayer graphene can be seen in the form of a faint residual feature in the AFM image (Figure 5a). This residue is suspected to consist of Au nanoparticles and is discussed in more detail in the next section. The calculated sheet resistance of this graphene device is 4.6 $k\Omega$ at $V_G = 0$ (measured resistance of ~31 $k\Omega$, which includes any contact resistance, was scaled with W/L of the device for $W = 885$ nm and $L = 6$ μm). This calculated sheet resistance is comparable to reported values (order 6.5 $k\Omega$) at $V_G = 0$.[24]

In addition to the NP residue, some graphene devices also showed cracks after processing. The AFM image in Figure 6 shows such damage to a device fabricated by careful alignment of the 5 μm gap parylene-C mask to an isolated monolayer graphene flake, so that MHA-masked electrodes were not needed. Such defects are also evident from the appearance of a D peak in the Raman spectrum of graphene after processing (Supporting Information, Figure S1). The corresponding output curves yield apparent sheet resistance values (7 to 9 $k\Omega$ for $W = 1.4$ μm at the narrowest point, $L = 3.6$ μm) that are higher than that for the device in Figure 5, which does not contain any cracks. Since the resistance increases past $V_G = 0$ to ~9 $k\Omega$ at $V_G = 15$ V, we may conclude that the Dirac point (charge neutrality point) is shifted at least +15 V, indicating that there is p-type doping in the graphene. It has been shown that graphene exhibits p-type doping behavior in ambient conditions due to physisorbed ambient impurities such as water[2] and oxygen.[25] Additionally, Au has been shown to have a hole-doping effect on graphene;[26] however, it remains inconclusive whether such an effect is being caused by the residual nanoparticles on these graphene devices.

Damage to Graphene during Processing. A series of trouble-shooting experiments was conducted to determine the
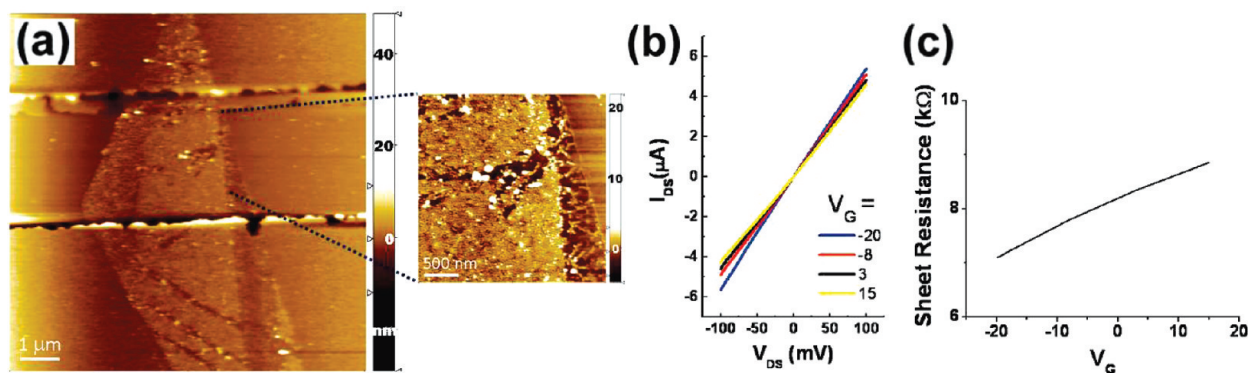

Figure 6. (a) AFM topography image of graphene device fabricated by direct alignment of parylene-C shadow mask to a DPN-defined monolayer flake. The graphene is shown between top and bottom Au electrodes, and the region that was overmasked with MHA can be discerned by the residual NPs on the surrounding SiO_2. The magnified image shows cracks in the graphene due to processing. (b) Corresponding output curves sweeping from $V_G = -20$ to 15 V. (c) Plot of apparent sheet resistance *versus* V_G, calculated from curves in (b).
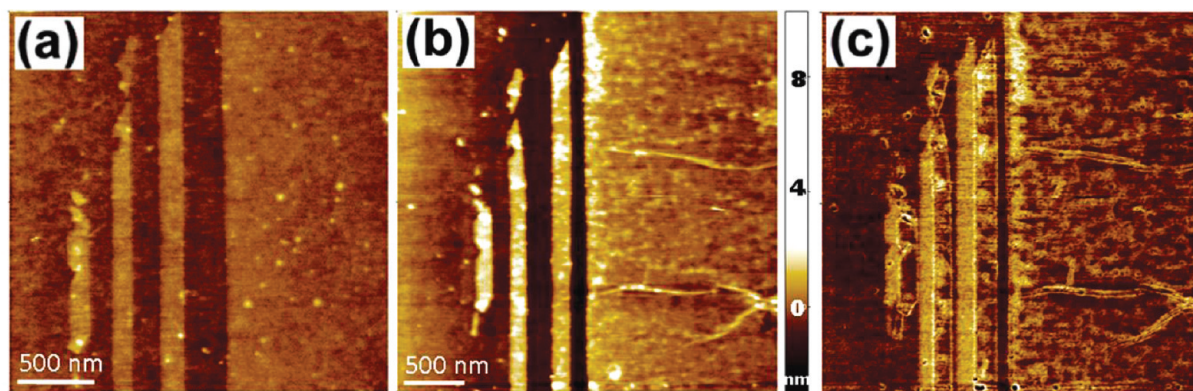
Figure 7. AFM images of graphene flakes before (a) and after (b,c) Au deposition and etching. The height scale is the same in (a) and (b). The shifting of the narrow graphene flakes to the right after processing is apparent in the phase image (c); the original position of the flakes is shown as a phase shift (lighter areas).

cause of these residual NPs and cracking in the graphene. The state of the graphene flakes was assessed after each processing step. To test whether there was any damage to the graphene after deposition of the 10 nm Au film and subsequent etching, an exfoliated graphene substrate was subjected to the aforementioned processing steps (without any DPN patterning). The results are shown in Figure 7, where cracks in the large flake and shifts in the narrow flakes are observed. Similar cracks have been observed in the literature with transfer printing of graphene using a Au film.[27] Although the cause of cracking was not discussed in that study, we hypothesize that these cracks may be due to high energy Au atoms impinging on the graphene surface and intercalating between the monolayer graphene and the underlying SiO_2 substrate, decoupling the graphene from the substrate.[26] This intercalation effect may serve to further weaken the graphene at certain defect sites, which have been shown to preferentially adsorb Au,[28] thereby making the flake more susceptible to fracture during wet etching. There is a higher frequency of damage to larger flakes (cracks are absent from the narrow flakes); this effect may be due to the incomplete decoupling of such large areas from the substrate surface, which leads to strain in the graphene as the decoupled parts shift and the other parts stick to the substrate during the wet Au etch. The decoupling of the graphene from the substrate is further supported by the shifting of the narrower graphene flakes on the substrate during Au etching (Figure 7c).

To verify that this effect is due to the Au deposition and not just the agitation during the wet etching step, another exfoliated graphene substrate was only exposed to the etching step. Supporting Information Figure S2 shows that no cracks were observed after this step; therefore, the combined Au deposition and subsequent etching steps lead to fracturing in graphene. Although the process step leading to macroscopic cracking has been identified, the origin and composition of the NP residue still remains unknown. A literature

search for AFM images of graphene devices revealed that the graphene may not be pristine and can contain some NP residue;[14,29] however, neither the cause nor the consequences of such surface contamination were discussed.

The NP residue observed on the devices remain after solvent rinsing and abate only after further Au etching of the graphene flakes (Supporting Information, Figure S3), suggesting that the NPs consist of Au. In order to pinpoint the source of this NP residue, a series of control experiments were performed on Au thin films deposited onto bare SiO_2 and exposed to O_2 plasma. Optical microscopy showed that the 10 nm Au films changed color from pink (Supporting Information, Figure S4a) to blue (Supporting Information, Figure S4b) upon O_2 plasma treatment, an effect that has been reported previously and attributed to oxidation of the Au; however, this color change is not completely reversible, as it should be after this unstable Au oxide reverts to metallic Au at room temperature after one day or faster upon heating of the Au film.[30]

AFM reveals that even after prolonged Au etching (13 min) and solvent rinsing, the NP residue (average height of 2 nm) still remains (Supporting Information, Figure S4d). This residue is not seen after etching Au films not exposed to O_2 plasma (Supporting Information, Figure S4c) or on bare SiO_2 exposed to O_2 plasma. Therefore, it is the O_2 plasma treatment of Au that causes this NP residue. If the NPs were just gold oxide, they should be reduced by the HCl in the Au etchant or heating to ~160 °C.[30] Therefore, the NPs are probably not gold oxide. Even after Au etching of the substrate one week later, the nanoparticle residue remained on the surface (Supporting Information, Figure S4d). Neither mechanical swabbing nor sonication in various solvents (toluene, acetone, or isopropyl alcohol) removes this NP residue. We hypothesize that this residue is composed of Au NPs complexed with carbonaceous contaminants (from the O_2 plasma chamber) that shield the Au NPs from etching.
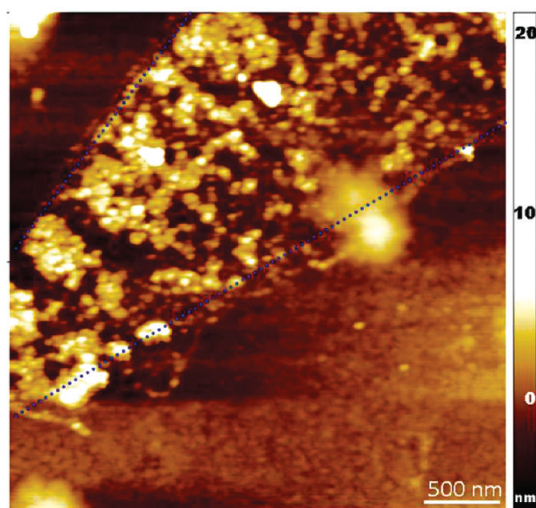
Figure 8. AFM topography image of monolayer graphene flake (within the dotted blue lines) defined with polystyrene as a sacrificial protective layer between graphene and the Au film. NP residue is on top of the graphene flake.

Mitigation of Nanoparticle Residue. In an attempt to reduce or eliminate this NP residue, a sacrificial polymer layer (polystyrene) was sandwiched between the graphene and Au thin film. This layer served two functions: (1) to reduce strain on graphene during Au deposition and etching by preventing the intercalation of Au atoms and (2) to facilitate removal of residual NPs after etching. Results indicate that the first function may be satisfied—cracks no longer appear in the graphene after processing; however, NP residue still remains on the surface (Figure 8).

In an attempt to facilitate removal of the NP residue *via* rinsing with polar solvents, poly(methyl methacrylate) (PMMA) was used as a sacrificial layer between a SiO_2 substrate and a gold film. After O_2 plasma treatment, Au etching, and sonication in acetone for 10 min, NP residue was still present (Supporting Information, Figure S5); however, the average height of this residue

was smaller than on the substrate without a sacrificial polymer layer (Supporting Information, Figure S4d). Further experiments revealed that a NP residue appears even for thicker Au films (40 nm) and shorter O_2 plasma exposure time (1 min) and lower power (50 W). It should be noted that although UV−ozone exposure would be a less harsh method for multilayer graphene removal, potentially avoiding this NP residue formation, it would take several hours, which would be inconvenient for most applications.

CONCLUSIONS

This study has demonstrated an application of DPN for fabricating nanoscale graphene devices and has identified process steps that may affect their electrical characterization. The sheet resistance of DPN-generated graphene devices was within the same order of magnitude as reported literature values. Contact resistance and fracture during the Au deposition and etching steps for defining monolayer graphene may have contributed to the slightly higher sheet resistance. However, fracture does not seem to be an issue with smaller graphene flakes such as nanoribbons, which are the eventual targets for fundamental studies of semiconducting behavior. Moreover, fracture can be prevented on larger flakes by using a sacrificial polymer layer between the graphene and the Au film. On the other hand, surface contamination resulting from DPN processing steps, and also seen in some prior reports using EBL, may prevent measurement of intrinsic material properties. This residue could not be eliminated through various postprocessing steps or even with the use of sacrificial polymer layers. Further studies need to be conducted to evaluate the effect of such contamination on measured properties. However, these composite Au−graphene nanostructures may be of interest for new catalytic and optoelectronic materials.[31]

METHODS

Substrate Preparation. Exfoliated graphene was deposited on heavily n-doped, hydrophobic SiO_2 using a previously published procedure.[2] The SiO_2 surface was rendered hydrophobic because previous studies with a hydrophilic surface from piranha cleaning showed delamination of graphene during solution processing. Therefore, a hydrophobic self-assembled monolayer (SAM) consisting of dodecyltriethoxysilane (Gelest, Morrisville, PA) was solution-deposited (1 vol % in toluene for 1 h) onto SiO_2 to promote graphene adhesion. Such SAMs on SiO_2 have been shown to reduce trapping sites for charge transport in other organic semiconductors such as pentacene, thereby increasing the charge carrier mobility.[32] DPN-templated SAMS have also been used to pattern graphene oxide sheets on substrates.[33]

DPN Masking. For DPN of MHA (16-mercaptohexadecanoic acid; Sigma-Aldrich, St. Louis, MO) masks, a thin Au film (10 nm) was thermally evaporated onto substrates containing graphene. Patterning (contact mode, set point 1.5 to 2 V) and imaging (contact and AC mode) were performed using an NSCRIPTOR DPN

system (NanoInk, Inc., Skokie, IL) at ambient temperature (26 ± 4 °C) and relative humidity (30−50%).

MHA was inked onto the diving-board cantilevers of type A Si_3N_4 probes (nominal spring constant 0.041 N/m) obtained from NanoInk, Inc. The AFM tips were dipped twice into 5 mM MHA in acetonitrile, once in deionized water, again into the MHA solution and finally into ethanol, with N_2 drying between the dipping steps. MHA-inked tips were used for rapid LFM imaging (speeds greater than 50 μm/s) of graphene flakes for contact registration and patterning verification. Discerning monolayer graphene regions under the Au film was difficult due to low contrast in the LFM images; therefore, the attached multilayer graphene was used to determine the location of monolayer graphene by comparing the scanned images to their optical counterparts.

Defining Monolayer Graphene. Once the monolayer graphene was masked by DPN of MHA, the substrate was exposed to a ferric nitrate/thiourea etch[18] (reagent volume 3 mL) for ~4 min at 100 rpm to etch unmasked gold and expose multilayer graphene. The substrate was then etched with O_2 plasma at 0.4 mbar, 80 W for 4 min to eliminate the multilayer graphene. This

was followed by a second Au etch to reveal the monolayer graphene flake.

Parylene-C Masking. Parylene-C shadow masks were used to pattern the macroscale Au electrodes (gap between electrodes at least 5 μm) on the substrate. A manual method was developed to align the channels in the parylene-C masks to graphene flakes: one end of the mask was secured with a tweezer and slowly lowered toward the substrate under 10× magnification in an optical microscope. Once alignment was verified through alignment markers, slight pressure was applied on the mask for lamination. Graphene device characterization with AFM and electrical testing followed the methods discussed in a previous report.[18]

Deposition of Sacrificial Polymer Layer. For experiments on the reduction of graphene fracture and nanoparticle residue, a protective, sacrificial polymer layer was spin-coated on the substrate before deposition of the thin Au film (10 nm). Polystyrene (PS, M_n = 88 000; Polymer Source Inc., Quebec, Canada) was used for exfoliated graphene since the SiO_2 was functionalized with a hydrophobic SAM. Substrates were flooded with solutions of PS/toluene (0.5 wt %), accelerated to 4000 rpm in less than 2 s, and left spinning for 60 s.[34] After definition of monolayer graphene, the sacrificial polymer was rinsed away with toluene.

Poly(methyl methacrylate) (PMMA, M_w ~120 000; Sigma-Aldrich) was evaluated for potential prevention or ease of removal of nanoparticle residue on bare SiO_2. A PMMA solution of 0.2 wt % in toluene was spin-coated onto substrates at 3000 rpm to yield a ~6 nm thick film.[35] Then Au thin films were deposited, exposed to O_2 plasma, and etched away. PMMA films were rinsed away with acetone.

Supporting Information Available: Optical images and Raman spectra of a graphene flake before and after processing to isolate the monolayer region (Figure S1). AFM topography images of exfoliated graphene on SiO_2 before and after exposure to the wet Au etchant (Figure S2). AFM topography images of a graphene device exposed to additional Au etching (Figure S3). Optical images of a Au film on SiO_2 before and after O_2 plasma treatment, and AFM images of SiO_2 after etching of a Au film without and with O_2 plasma treatment (Figure S4). AFM image of SiO_2 after removal of sacrificial PMMA layer (Figure S5). This material is available free of charge *via* the Internet at http://pubs.acs.org.

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